

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Docket No: Q78644

Yasunori BITO

Appln. No.: Unknown

Confirmation No.: Unknown

Group Art Unit: Unknown

Filed: November 25, 2003

Examiner: Unknown

For: HETEROJUNCTION FIELD EFFECT TYPE SEMICONDUCTOR DEVICE HAVING HIGH GATE TURN-ON VOLTAGE AND LOW ON-RESISTANCE AND ITS MANUFACTURING METHOD

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached PTO/SB/08 A & B (modified) form and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

One copy of each of the listed documents is submitted herewith.

1. Y. Bito et al., "64% Efficiency Enhancement-Mode Power Heterojunction Fet for 3.5 V Li-ION Battery Operated Personal Digital Cellular Phones", 1998 IEEE MTT-S Int. Microwave Symp-Dig., June 1998, pp. 439-442 with Abstract.
2. S. Wada et al., "0.1- μm p⁺-GaAs Gate HJFET's Fabricated Using Two-Step Dry-Etching and Selective MOMBE Growth Techniques", IEEE Transactions on Electron Devices, Vol. 45, No. 6, June 1998, pp. 1383-1389 with Abstract.

Yasunori BITO
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INFORMATION DISCLOSURE STATEMENT

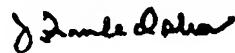
3. K. Nishii et al., "High Current/gm Self-Aligned PJ-HFET of Completely Enhancement-Mode Operation", Extended Abstracts of the 1998 International Conference on Solid-State Devices and Materials, 1998, pp. 396-397.

The present Information Disclosure Statement is being filed: (1) No later than three months from the application's filing date; (2) Before the mailing date of the first Office Action on the merits (whichever is later); or (3) Before the mailing date of the first Office Action after filing a request for continued examination (RCE) under §1.114, and therefore, no Statement under 37 C.F.R. § 1.97(e) or fee under 37 C.F.R. § 1.17(p) is required.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,



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WASHINGTON OFFICE

23373

CUSTOMER NUMBER

Date: November 25, 2003

Substitute for Form 1449 A & B/PTO <u>INFORMATION DISCLOSURE</u> <u>STATEMENT BY APPLICANT</u> <i>(use as many sheets as necessary)</i>				<i>Complete if Known</i>	
				Application Number	Unknown
				Confirmation Number	Unknown
				Filing Date	November 25, 2003
				First Named Inventor	Yasunori BITO
				Art Unit	Unknown
Examiner Name	Unknown				
Sheet	1	of	1	Attorney Docket Number	Q78644

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		Number	Kind Code ² (if known)		
		US			
		US			
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FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Translation ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)			

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	Translation ⁶
		Y. Bito et al., "64% Efficiency Enhancement-Mode Power Heterojunction Fet for 3.5 V Li-ION Battery Operated Personal Digital Cellular Phones", 1998 IEEE MTT-S Int. Microwave Symp-Dig., June 1998, pp. 439-442 with Abstract.	
		S. Wada et al., "0.1- μ m p ⁺ -GaAs Gate HJFET's Fabricated Using Two-Step Dry-Etching and Selective MOMBE Growth Techniques", IEEE Transactions on Electron Devices, Vol. 45, No. 6, June 1998, pp. 1383-1389 with Abstract.	
		K. Nishii et al., "High Current/gm Self-Aligned PJ-HFET of Completely Enhancement-Mode Operation", Extended Abstracts of the 1998 International Conference on Solid-State Devices and Materials, 1998, pp. 396-397.	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²See Kind Codes of USPTO Patent Documents at www.uspto.gov, MPEP 901.04 or in the comment box of this document. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to indicate here if English language Translation is attached.